

POPL 2017
Paris

A Promising Semantics for Relaxed-Memory Concurrency

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Relaxed-Memory Concurrency

- **Semantics of multi-threaded programs?**
 - Sequential consistency (SC): simple but **expensive**
- **Relaxed memory models (C/C++, Java)**
 - Many consistency modes (cost vs. consistency tradeoff)
 - **Open problem:** what is the “**right**” semantics?

“Right” Concurrency Semantics?

- **Conflicting goals of “masters”**
- **Compiler/hardware:** validating optimizations (e.g. reordering, merging)
- **Programmer:** supporting reasoning principles (e.g. DRF theorem, program logic)

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Key problem: “out-of-thin-air”

“Out-of-thin-air” problem (1/3)

Load-Buffering (LB)

Thread 1

$a = X$

$Y = a$

($a=b=42?$)

Thread 2

$b = Y$

$X = 42$

“Out-of-thin-air” problem (1/3)

Load-Buffering (LB)

Registers

Thread 1

$a = X$

$Y = a$

Thread 2

$b = Y$

$X = 42$

($a=b=42?$)

“Out-of-thin-air” problem (1/3)

Load Interfering (LB)

Registers

Shared Locations

Thread 1

Thread 2

$a = X$

$b = Y$

$Y = a$

$X = 42$

($a=b=42?$)

“Out-of-thin-air” problem (1/3)

Load Ordering (LB)

Registers

Shared Locations

Thread 1

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$a = X$

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$X = 42$

CII
Relaxed

($a=b=42?$)

“Out-of-thin-air” problem (1/3)

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Allowed by reordering
(Power/ARM)

$X = 42$

$b = Y$

“Out-of-thin-air” problem (1/3)

Load-Buffering (LB)

Thread 1

a = X
Y = a

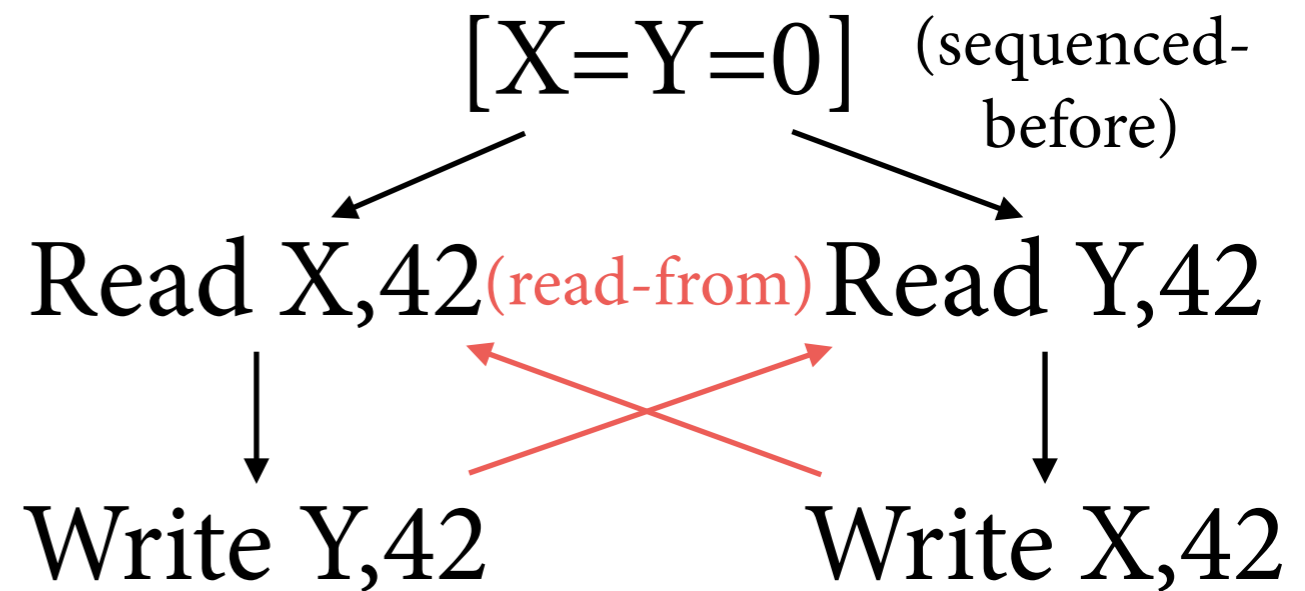
(a=b=42?)

Thread 2

b = Y
X = 42

Allowed by reordering
(Power/ARM)

X = 42
b = Y



Allowed by justification
(C/C++)

“Out-of-thin-air” problem (1/3)

Load-Buffering (LB)

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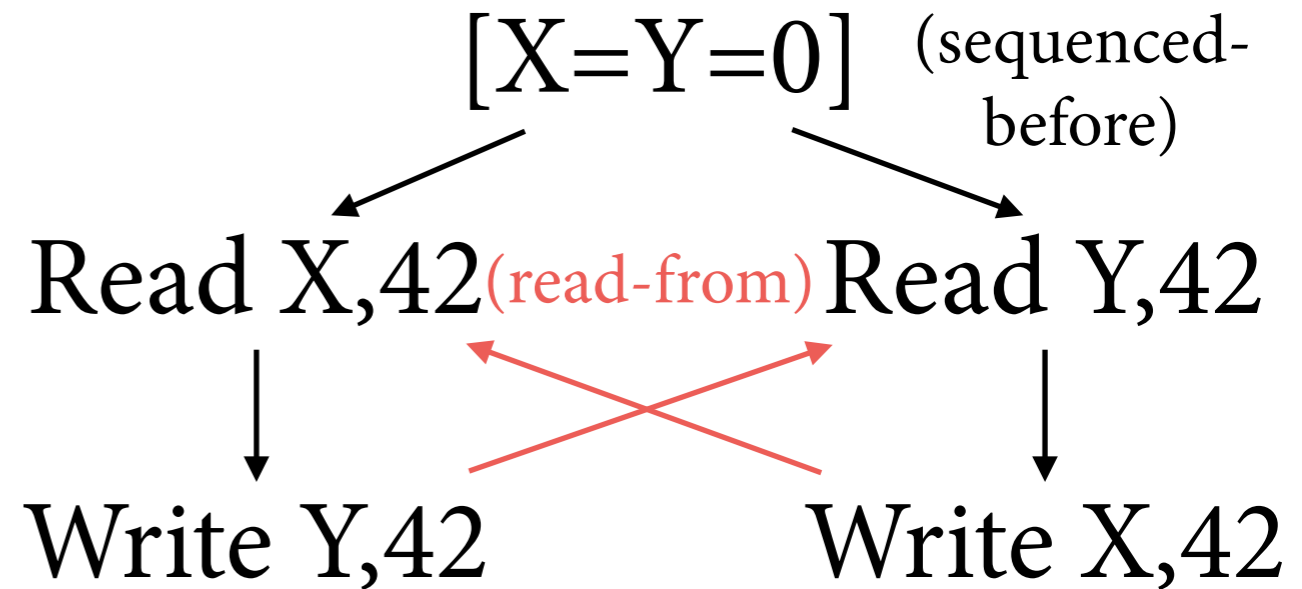
(a=b=42?)

Thread 2

b = Y
X = 42

Allowed by reordering
(Power/ARM)

X = 42
b = Y



Allowed by justification
(C/C++)

Justification is
too loose!

“Out-of-thin-air” problem (2/3)

Classic Out-of-thin-air (OOTA)

Thread 1

$a = X$

$Y = a$

($a=b=42?$)

Thread 2

$b = Y$

$X = b$

“Out-of-thin-air” problem (2/3)

Classic Out-of-thin-air (OOTA)

Thread 1

$a = X$

$Y = a$

Thread 2

$b = Y$

$X = b$

($a=b=42?$)

should be **forbidden**
42 is out-of-thin-air!

Reasoning principles
(e.g. invariant $a=b=X=Y=0$)

“Out-of-thin-air” problem (2/3)

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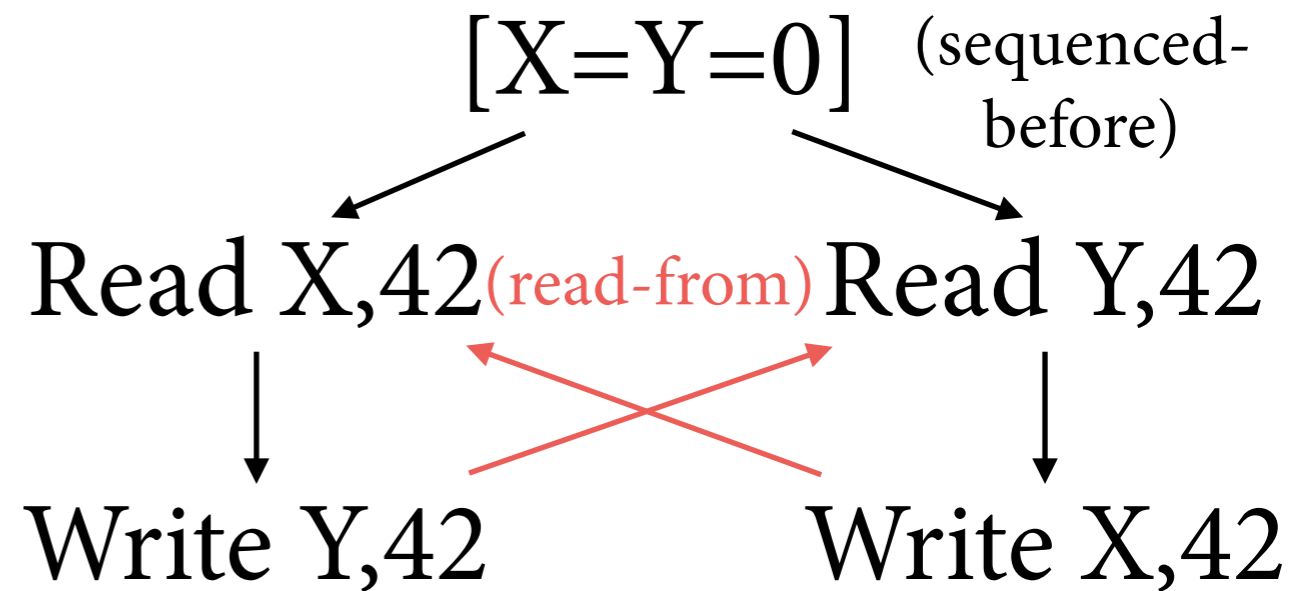
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$b = Y$

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Reasoning principles
(e.g. invariant $a=b=X=Y=0$)



Allowed by justification
w/ same graph (C/C++)

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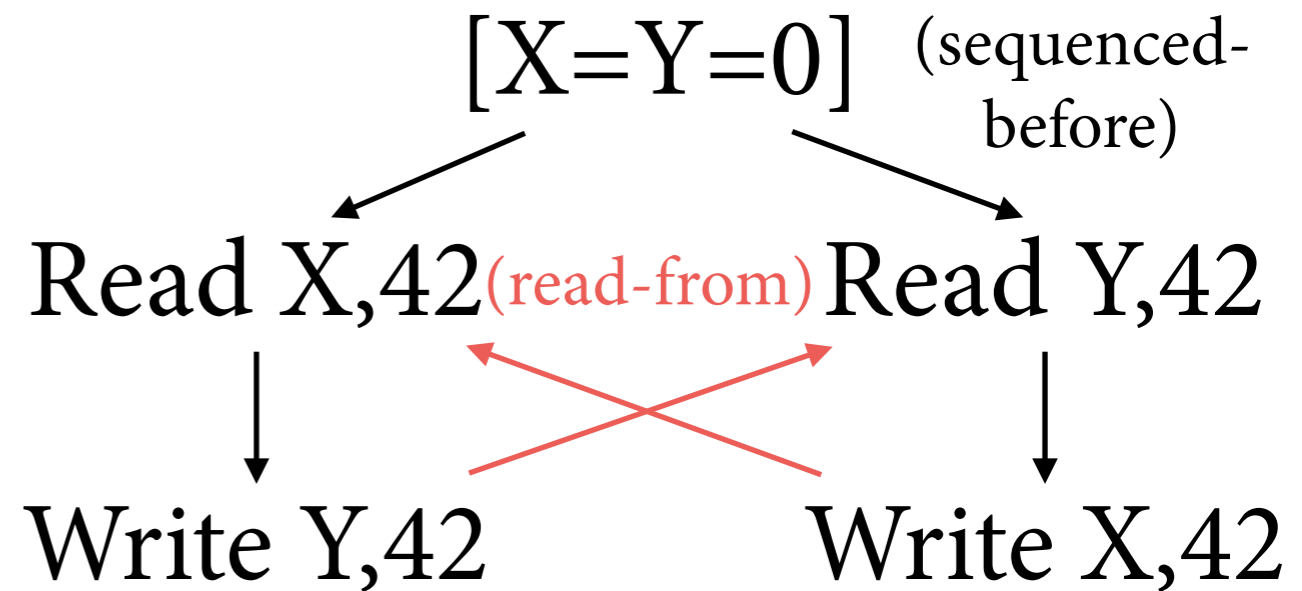
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Thread 2

b = Y
X = b

should be **forbidden**
42 is out-of-thin-air!

Reasoning principles
(e.g. invariant $a=b=X=Y=0$)



Allowed by justification
w/ same graph (C/C++)

What does
hardware do?

“Out-of-thin-air” problem (3/3)

Tracking Syntactic Dependency?

Thread 1

$a = X$

$Y = a$

($a=b=42?$)

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$Y = a$

($a=b=42?$)

Thread 2

$b = Y$

$X = b$ (dep.)

“Out-of-thin-air” problem (3/3)

Tracking Syntactic Dependency?

Thread 1

$a = X$

$Y = a$

($a=b=42?$)

Thread 2

$b = Y$

$X = 42$

allowed
in hardware

Thread 1

$a = X$

$Y = a$

($a=b=42?$)

Thread 2

~~$b = Y$~~

~~$X = b$~~ (dep.)

forbidden
in hardware

“Out-of-thin-air” problem (3/3)

Tracking Syntactic Dependency?

Thread 1

$a = X$

$Y = a$

($a=b=42?$)

Thread 2

$b = Y$

$X = b+42-b$

Thread 1

$a = X$

$Y = a$

($a=b=42?$)

Thread 2

~~$b = Y$~~
 ~~$X = b$~~ (dep.)

forbidden
in hardware

“Out-of-thin-air” problem (3/3)

Tracking Syntactic Dependency?

Thread 1

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Thread 2

~~$b = Y$~~

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forbidden
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forbidden
in hardware

could be optimized to “42”,
should be allowed in PL

“Out-of-thin-air” problem (3/3)

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could be optimized to “42”,
should be allowed in PL

Syntactic approach
doesn't work for PL!

“Out-of-thin-air” problem (3/3)

“A major open problem for PL semantics”
(Batty et al. ESOP 2015)

Thread 1

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forbidden
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 $X = b$ (dep.)

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could be optimized to “42”,
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Promising Semantics

- Solving the **out-of-thin-air problem**
- Supporting **optimizations & reasoning principles**
- Covering most **C/C++ concurrency** features
- **Operational semantics w/o undefined behavior**

- Most results are **verified in Coq**
<http://sf.snu.ac.kr/promise-concurrency>



Key Idea: Promises

- A thread can **promise** to write $X=V$ in the future, after which **other threads can read** $X=V$.
- To avoid OOTA, the promising thread must **certify** that it can write $X=V$ **in isolation**.

Key Idea: Promises

Thread 1

$a = X$

$Y = a$

Thread 2

$b = Y$

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$a = X$

$Y = a$

Thread 2

$b = Y$

$X = 42$

$X=42$ promised

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Y = a

Thread 2

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Certified:
T2 in isolation

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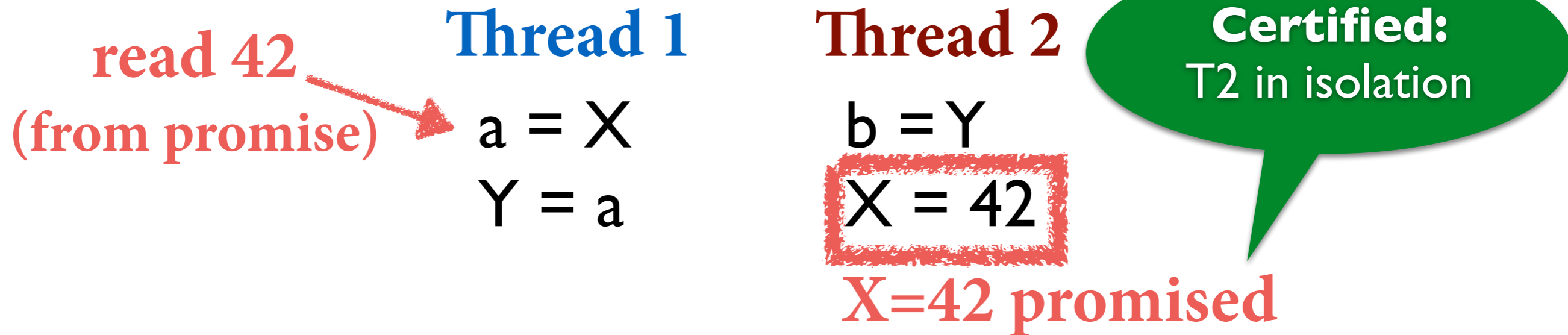
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$X=42$ promised

Certified:
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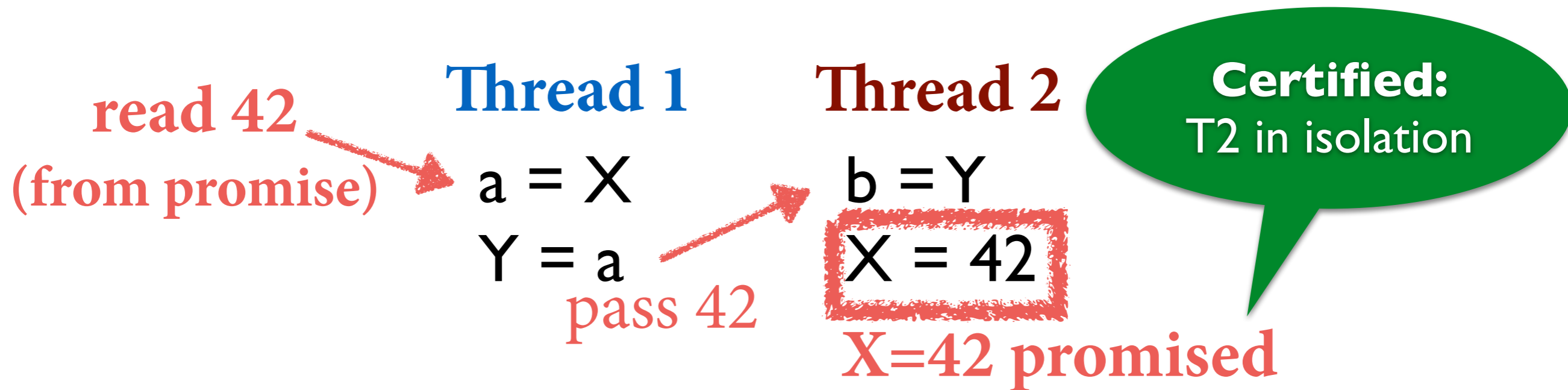
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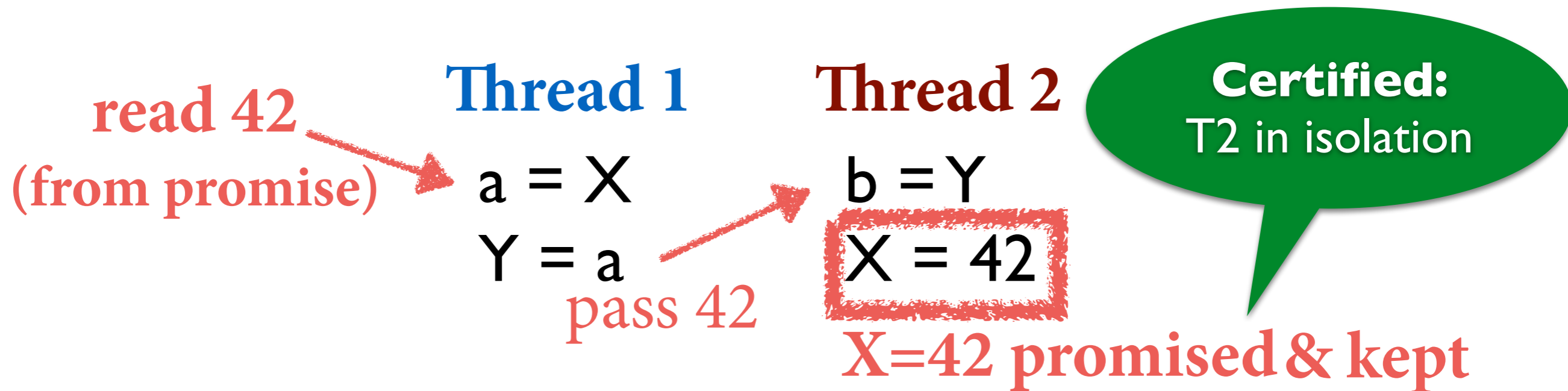
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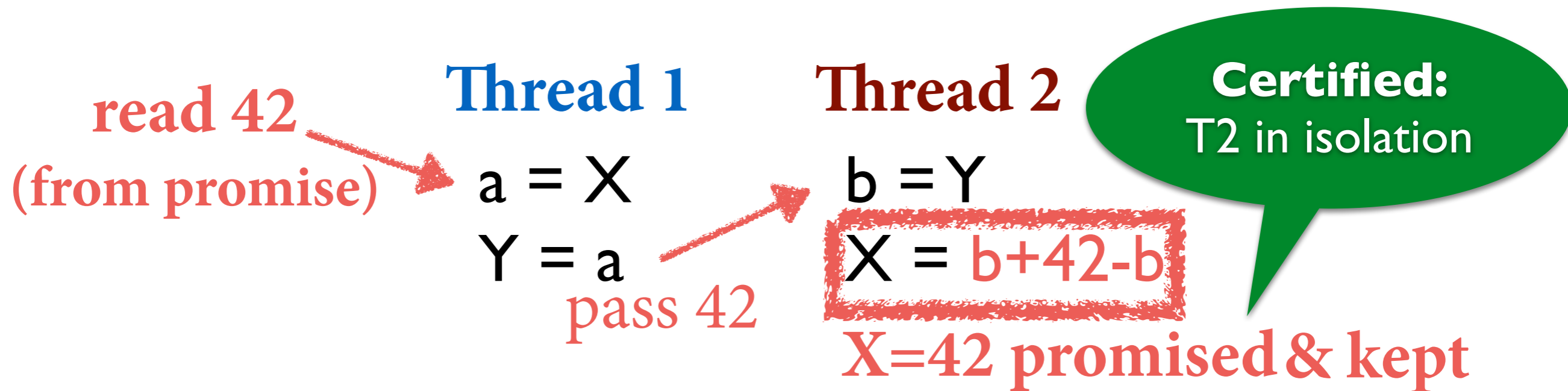
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Key Idea: Promises

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Y = a

Thread 2

b = Y

X = b

cannot promise X=42

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Promises: “Semantic Solution” to OOTA

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$Y = a$

Thread 2

$b = Y$

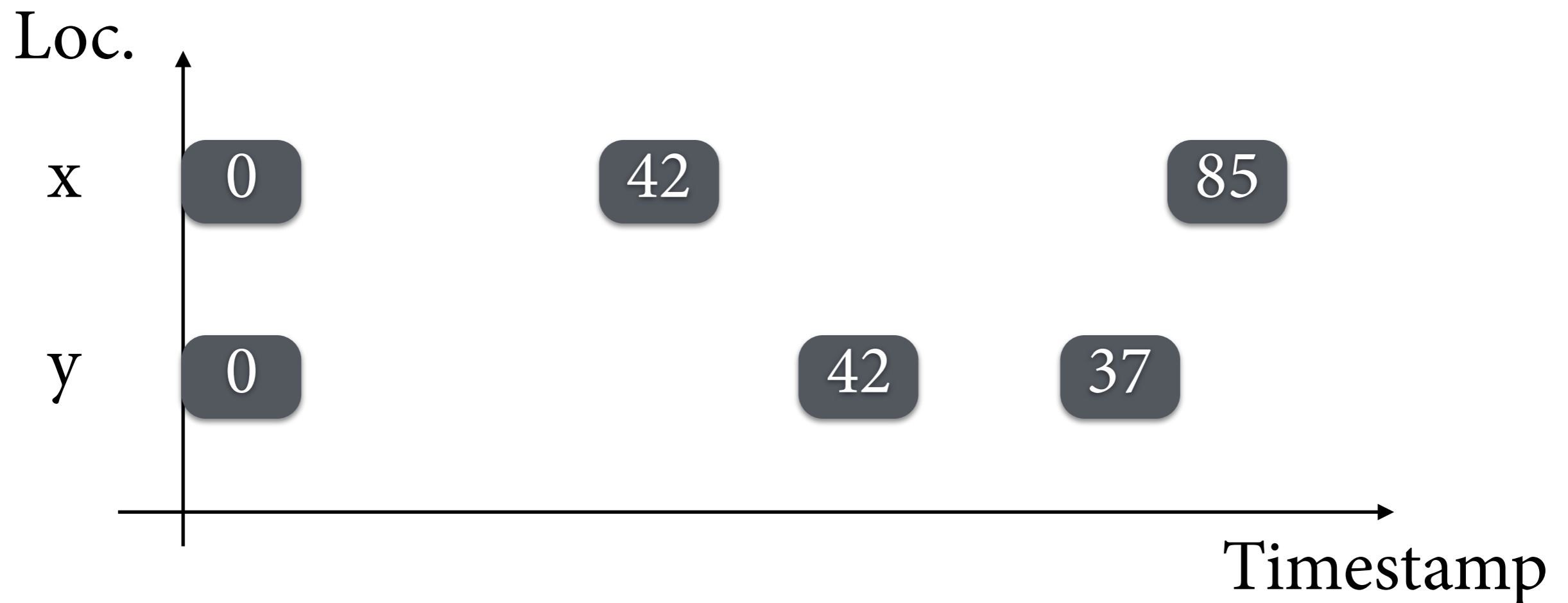
$X = b$

cannot promise $X=42$

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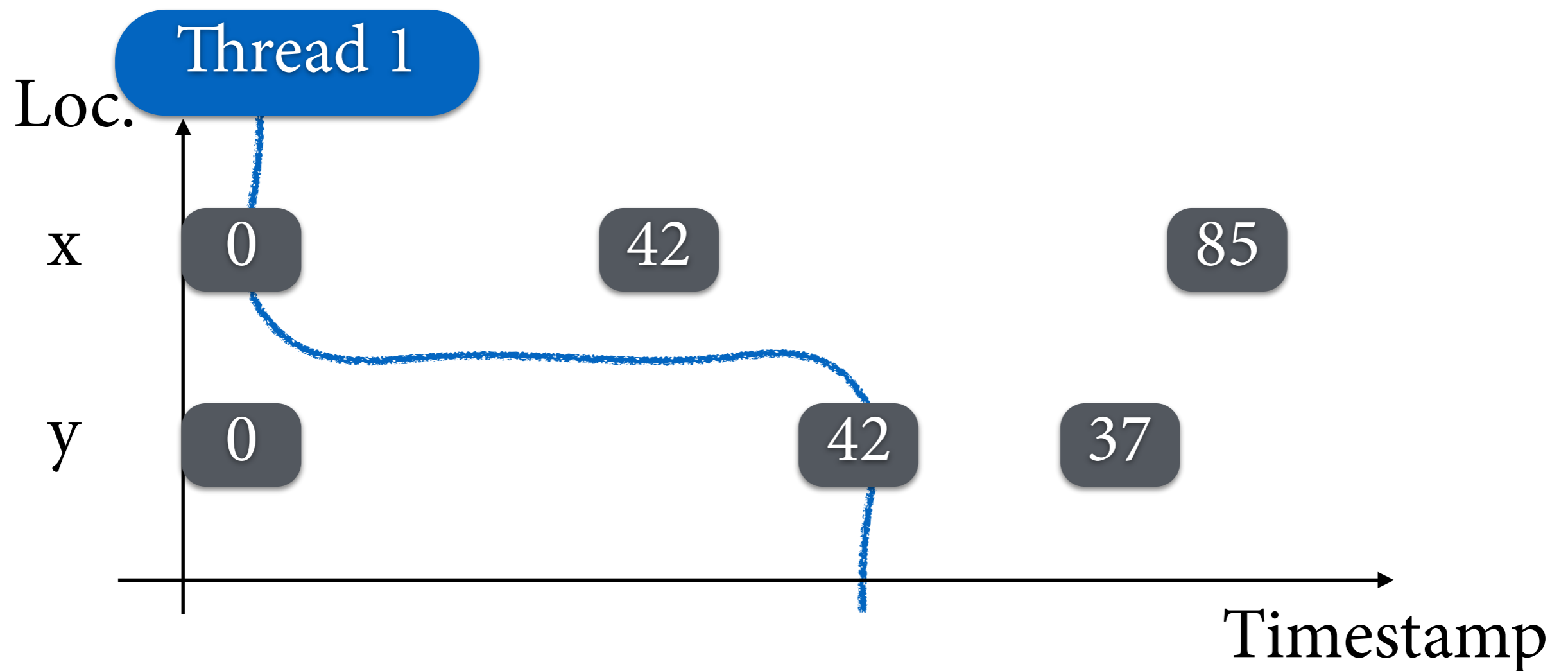
Basis: Operational Semantics

- Memory: pool of **messages** (loc, val, timestamp)
- Per-thread **view** on the memory



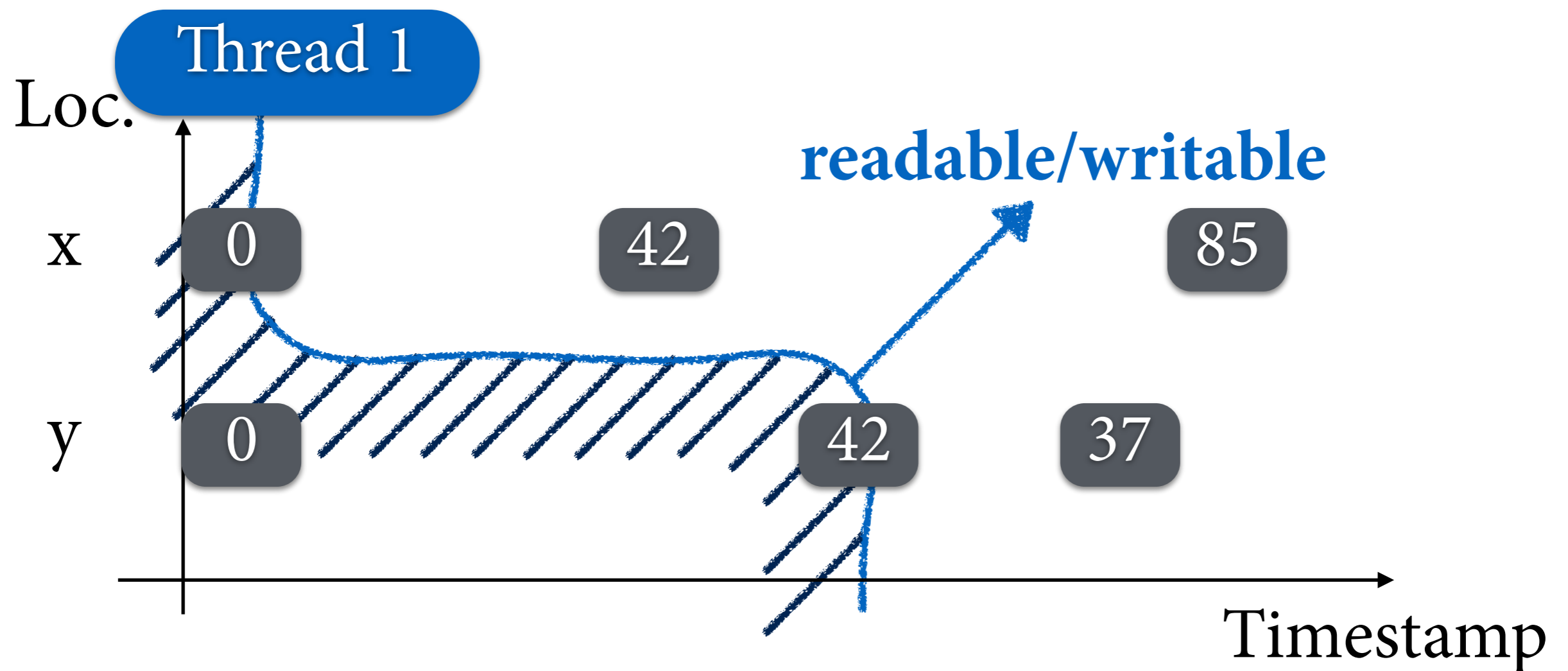
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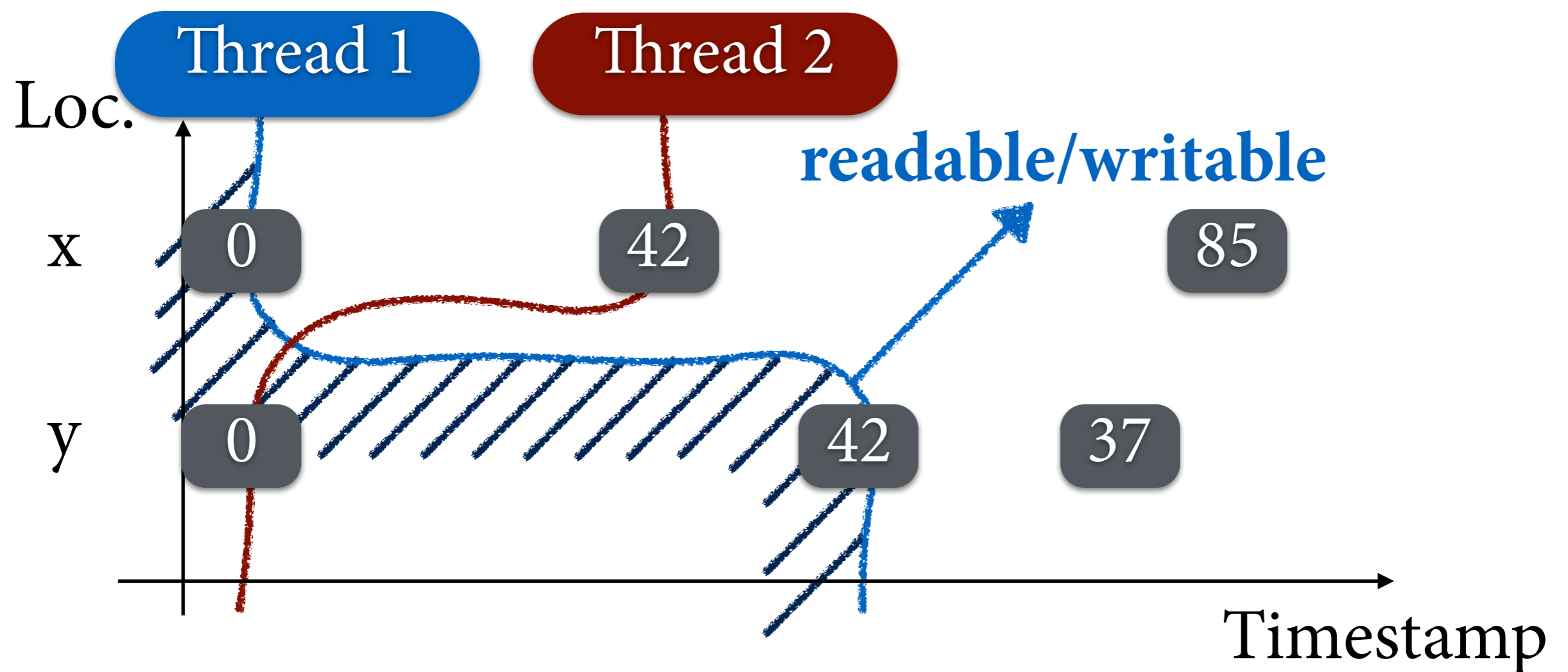
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- Memory: pool of **messages** (loc, val, timestamp)
- Per-thread **view** on the memory



Example (1/3)

Store Buffering

Thread 1

→ $Y = 42$
 $a = X$

Thread 2

→ $X = 42$
 $b = Y$

(allowed: $a=b=0$)



Example (1/3)

Store Buffering

Thread 1

→ $Y = 42$
 $a = X$

Thread 2

→ $X = 42$
 $b = Y$

(allowed: $a=b=0$)

→
reorderable
(x86/Power/ARM)

$b = Y$
 $X = 42$



Example (1/3)

Store Buffering

Thread 1

→ $Y = 42$
 $a = X$

Thread 2

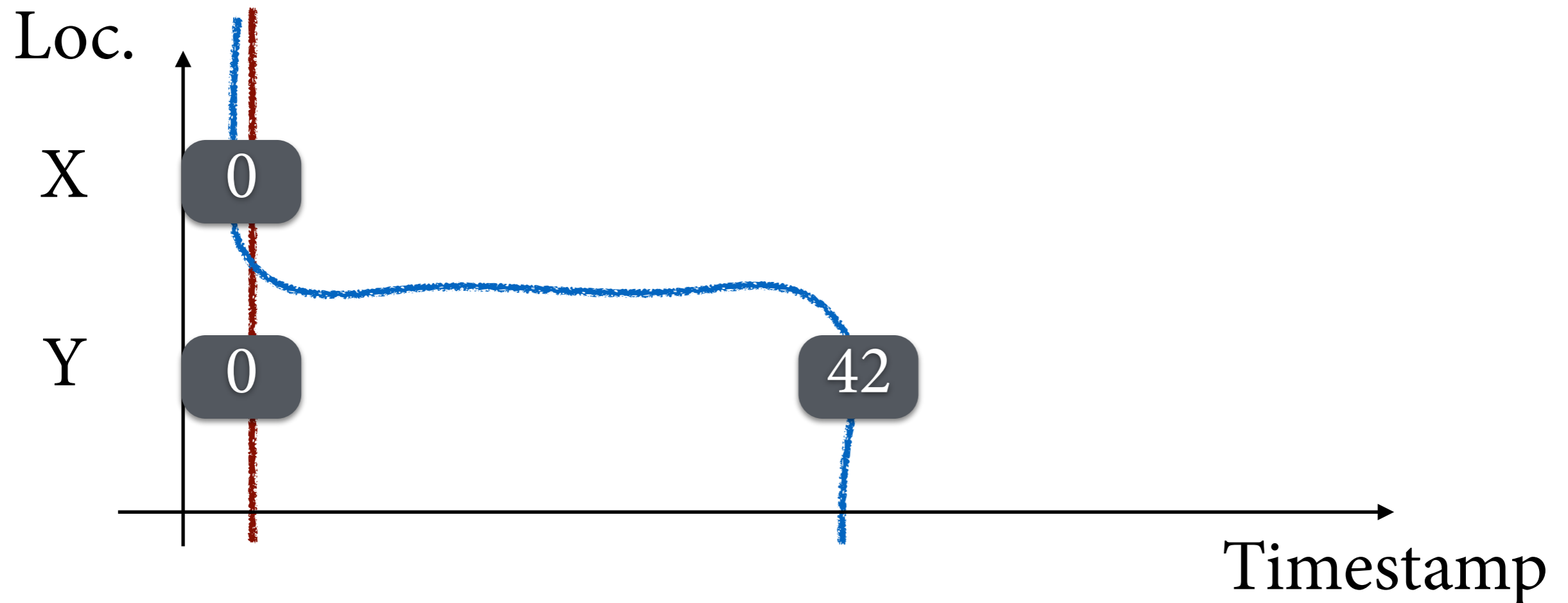
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Example (1/3)

Store Buffering

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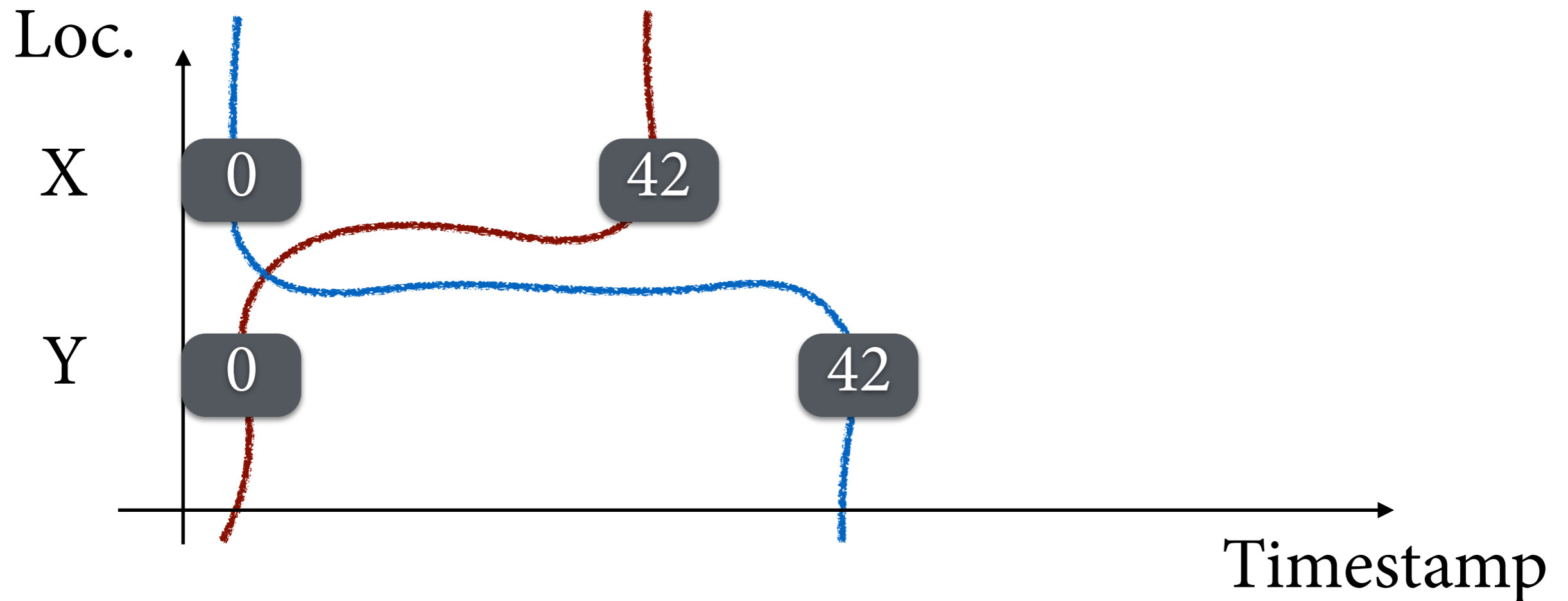
Thread 2

→ $X = 42$
 $b = Y$

(allowed: $a=b=0$)

→
reorderable
(x86/Power/ARM)

$b = Y$
 $X = 42$



Example (1/3)

Store Buffering

Thread 1

$Y = 42$
 $a = X$



Thread 2

$X = 42$
 $b = Y$



(allowed: $a=b=0$)



reorderable

(x86/Power/ARM)

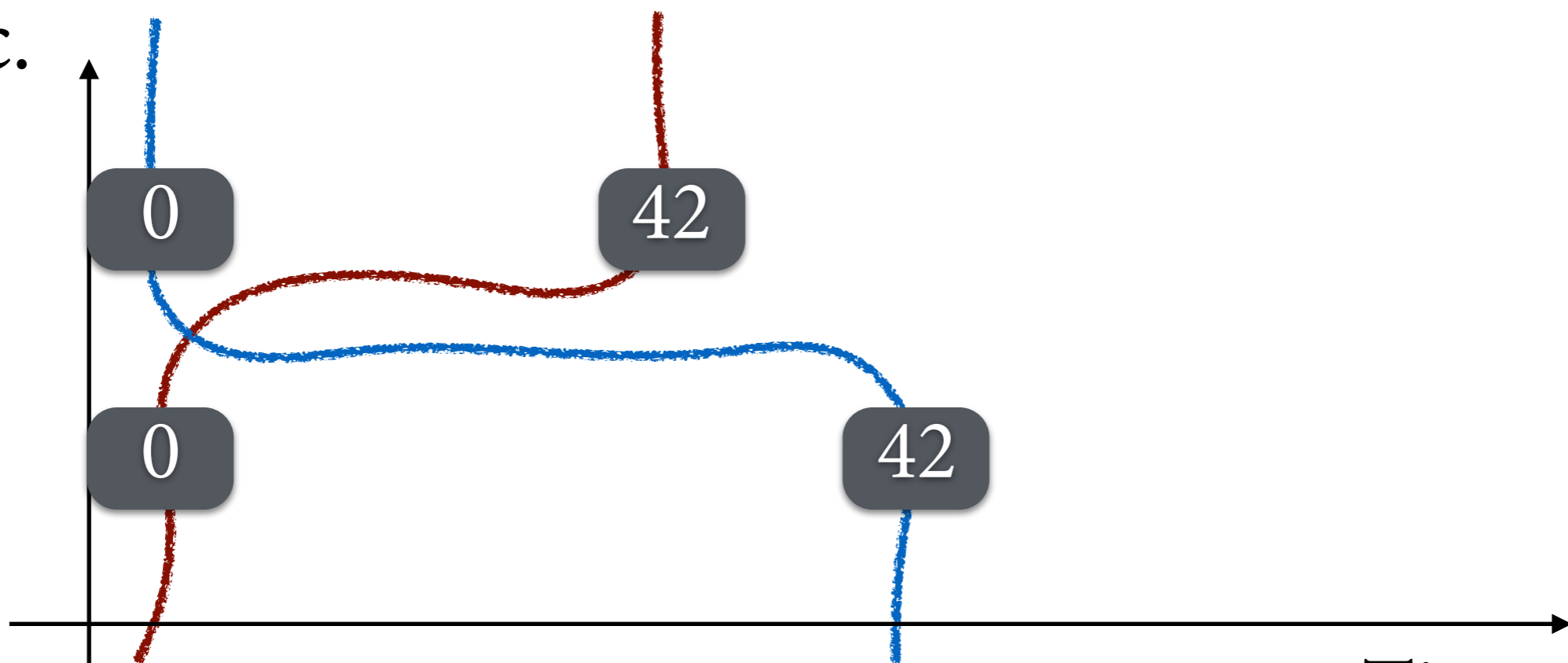
$b = Y$

$X = 42$

Loc.

X

Y



Timestamp

Example (1/3)

Store Buffering

Thread 1

$Y = 42$

$a = X$



Thread 2

$X = 42$

$b = Y$



(allowed: $a=b=0$)



reorderable

(x86/Power/ARM)

$b = Y$

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Loc.

X

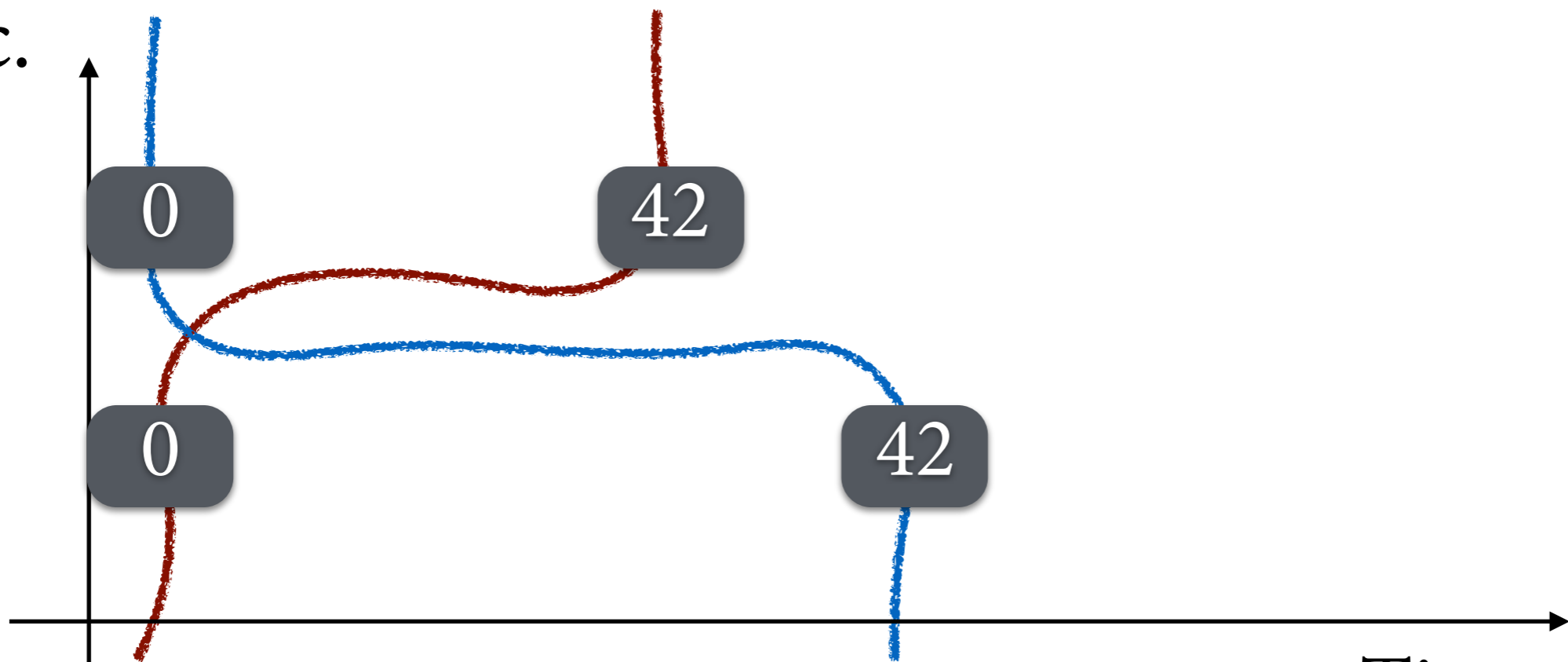
0

42

Y

0

42



Timestamp

Example (2/3)

Load Buffering (LB)

Thread 1



$a = X$

$Y = a$

Thread 2



$b = Y$

$X = 42$

(allowed: $a=b=42$)



Example (2/3)

Load Buffering (LB)

Thread 1



$a = X$

$Y = a$

Thread 2



$b = Y$

$X = 42$

(allowed: $a=b=42$)

Loc.

X

0

Y

0

Thread 2's
promise

42

Timestamp

Example (2/3)

Load Buffering (LB)

Thread 1



$a = X$

$Y = a$

Thread 2



$b = Y$

$X = 42$

(allowed: $a=b=42$)

Loc.

X

0

Y

0

Thread 2's
promise

42

Thread 2 should be
able to write it
in isolation

Timestamp

Example (2/3)

Certification

Thread 2



$b = Y$

$X = 42$



Example (2/3)

Certification

Thread 2

→ $b = Y$
 $X = 42$



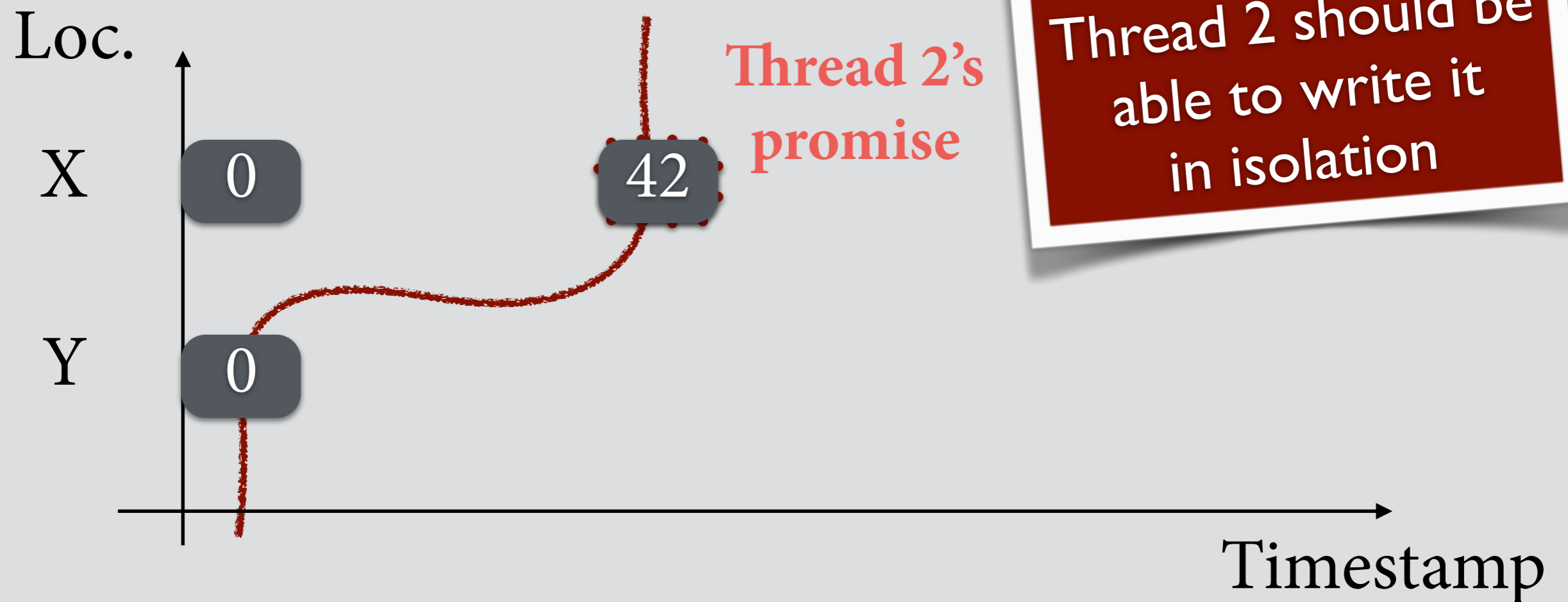
Example (2/3)

Certification

Thread 2

$b = Y$

→ $X = 42$



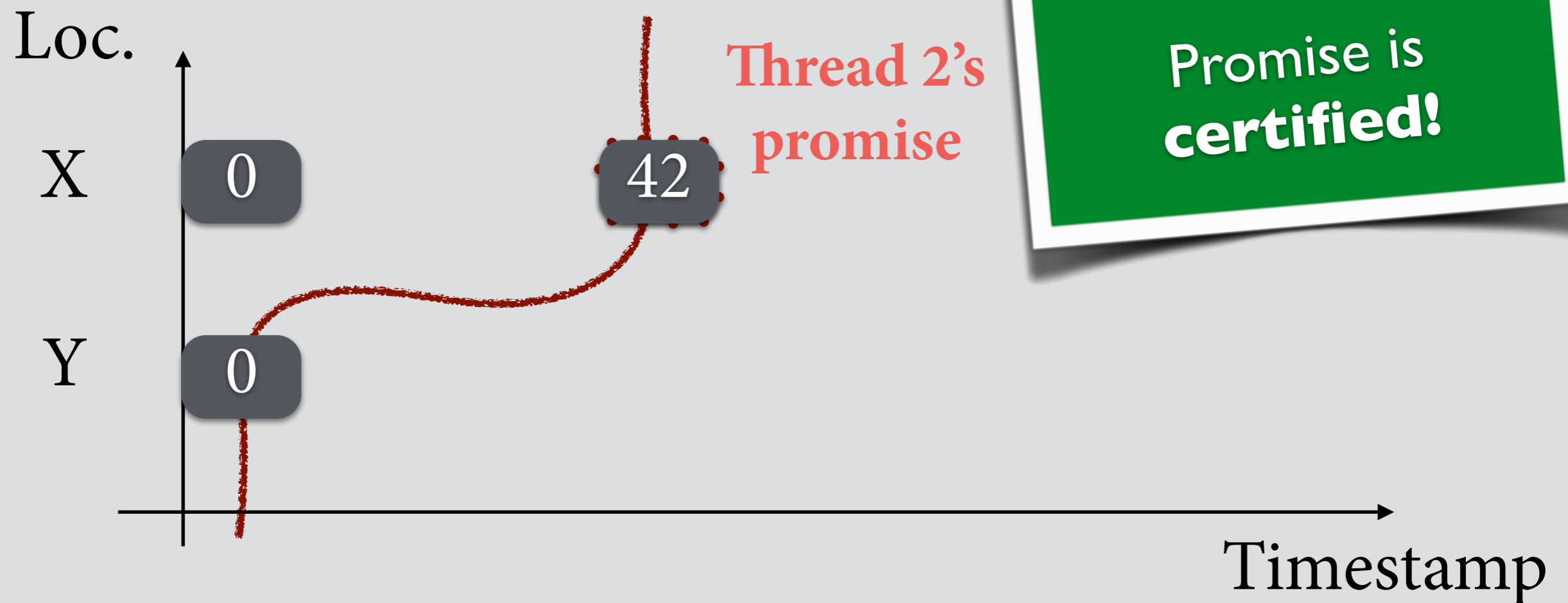
Example (2/3)

Certification

Thread 2

$b = Y$

$\rightarrow X = 42$



Example (2/3)

Load Buffering (LB)

Thread 1



$a = X$

$Y = a$

Thread 2



$b = Y$

$X = 42$

(allowed: $a=b=42$)

Loc.

X

0

Y

0

Thread 2's
promise

42

Promise is
certified!

Timestamp

Example (2/3)

Load Buffering (LB)

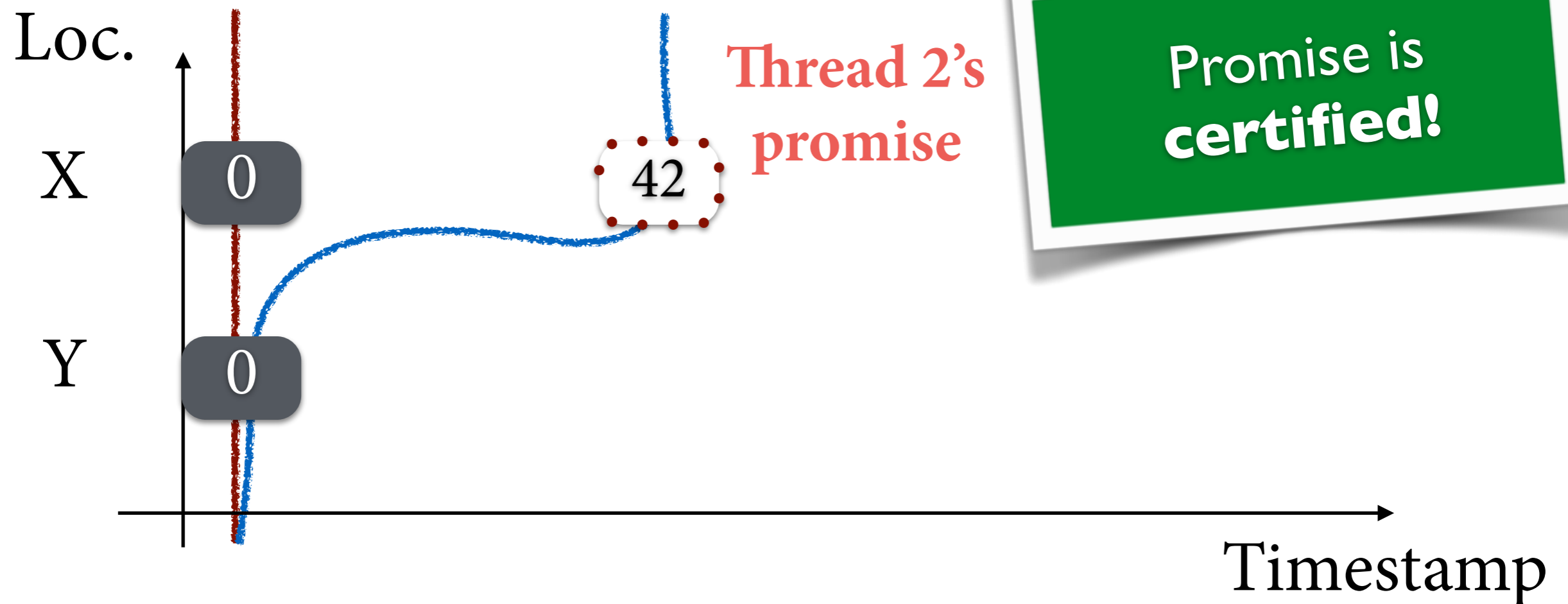
Thread 1

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 $Y = a$

Thread 2

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Example (2/3)

Load Buffering (LB)

Thread 1

$a = X$

$Y = a$



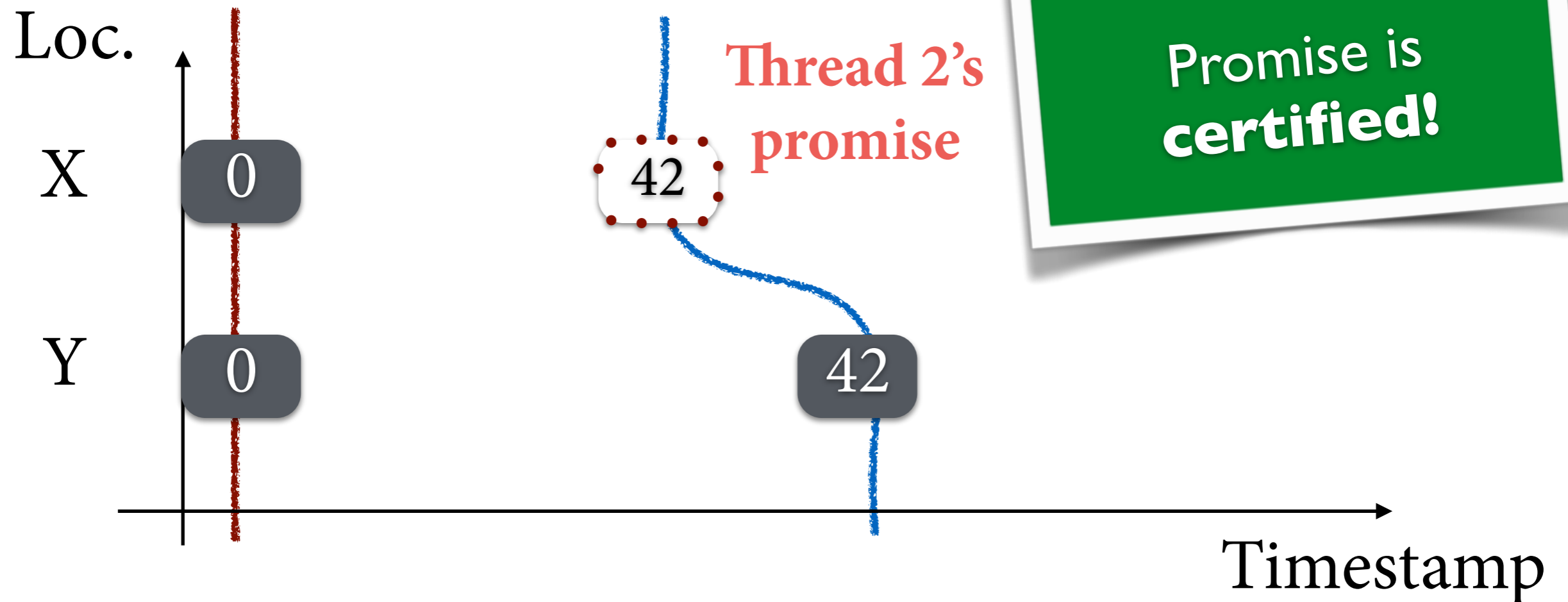
Thread 2



$b = Y$

$X = 42$

(allowed: $a=b=42$)



Example (2/3)

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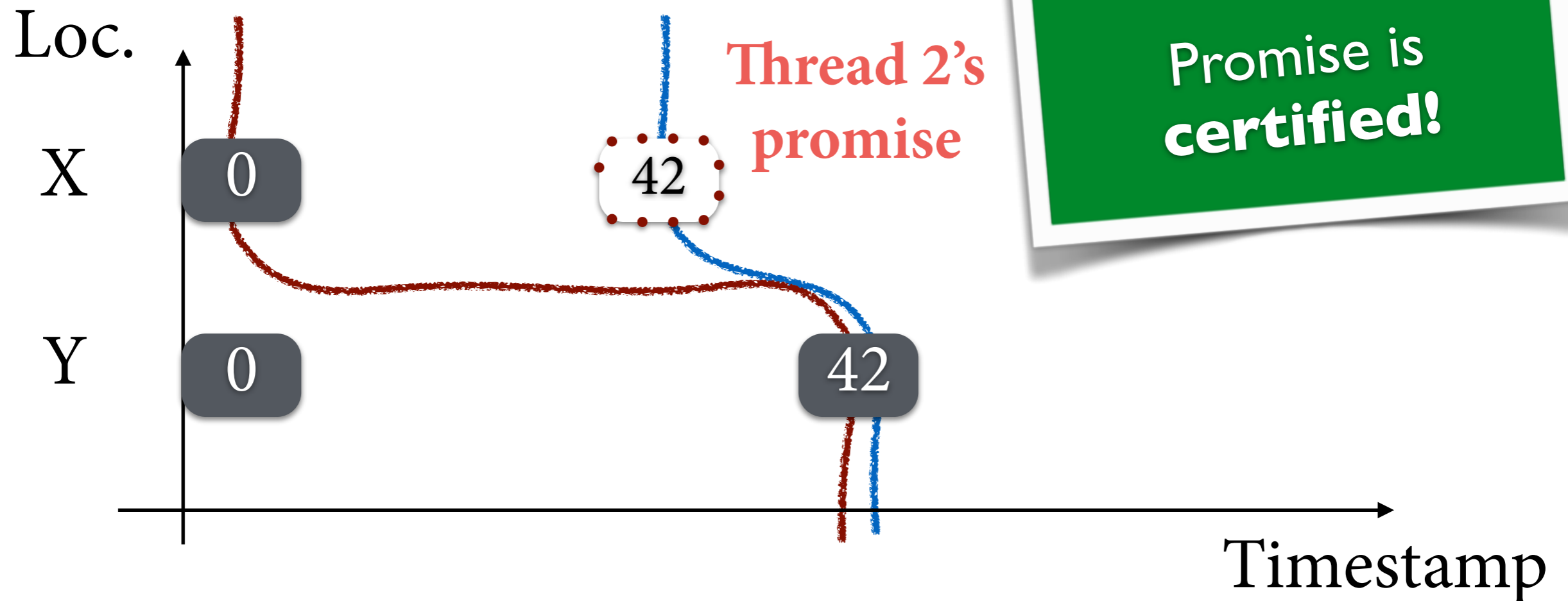
Thread 2

$b = Y$

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(allowed: $a=b=42$)



Example (2/3)

Load Buffering (LB)

Thread 1

$a = X$

$Y = a$



Thread 2

$b = Y$

$X = 42$



(allowed: $a=b=42$)

Loc.

X

0

42

Y

0

42

Thread 2's
promise

Promise is
certified!

Timestamp

Example (2/3)

Load Buffering (LB)

Thread 1

$a = X$

$Y = a$



Thread 2

$b = Y$

$X = b + 42 - b$



(allowed: $a=b=42$)

false dependency makes no difference!

Promise is certified!

Loc.

X

0

42

Y

0

42

Thread 2's promise

Timestamp

Example (3/3)

Classic Out-of-thin-air (OOTA)

Thread 1



$a = X$

$Y = a$

Thread 2



$b = Y$

$X = b$

(forbidden: $a=b=42$)



Example (3/3)

Classic Out-of-thin-air (OOTA)

Thread 1



$a = X$

$Y = a$

Thread 2



$b = Y$

$X = b$

(forbidden: $a=b=42$)

Loc.

X

0

Y

0

Thread 2's
promise?

42

Timestamp

Example (3/3)

Classic Out-of-thin-air (OOTA)

Thread 1

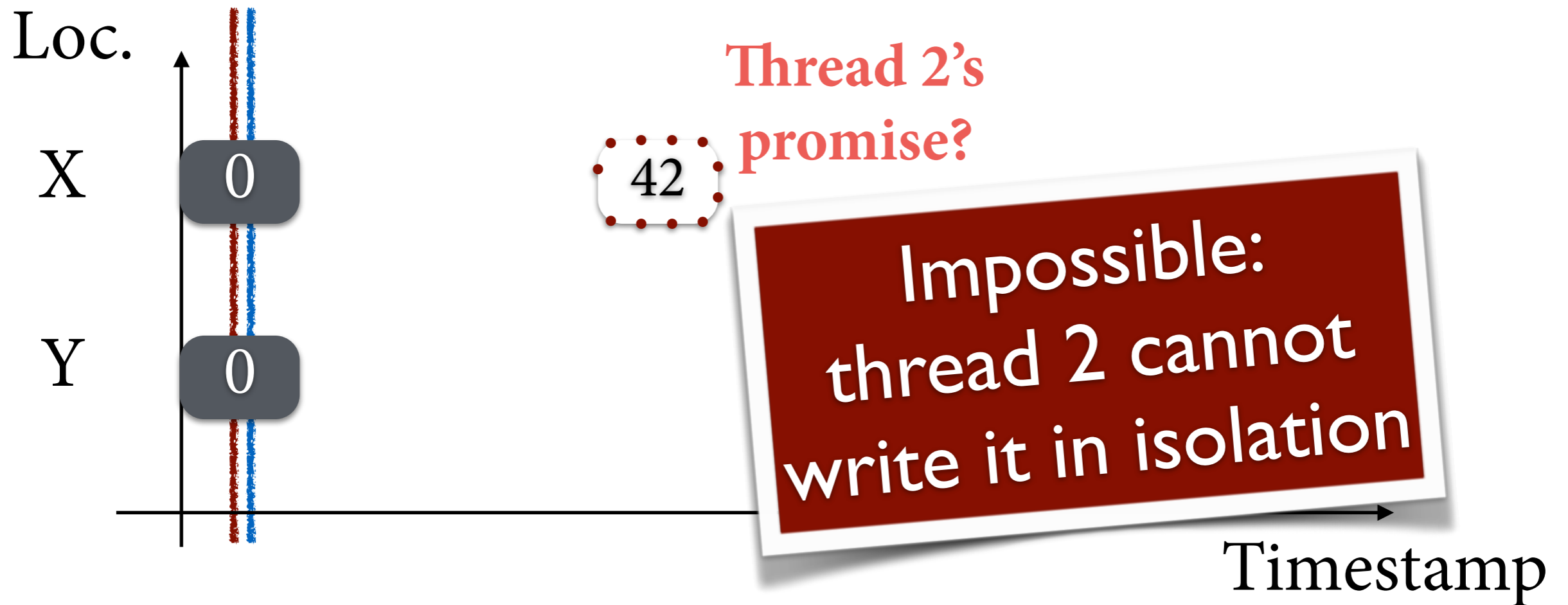
→

$a = X$
 $Y = a$

Thread 2 (forbidden: $a=b=42$)

→

$b = Y$
 $X = b$



Promises: "Semantic Solution" to OOTA

Thread 1



$a = X$

$Y = a$

Thread 2



$b = Y$

$X = b$

(forbidden: $a=b=42$)

Loc.

X

0

Y

0




Thread 2's
promise?

42

Impossible:
thread 2 cannot
write it in isolation




Timestamp

Compiler/HW Optimizations

- **Operational semantics** for C/C++ concurrency:
plain/relaxed/release/acquire r/w/u/fence, SC fence
- **Compiler optimizations** 
(reordering, merging, dead code elim., ...)
- **Compilation to x86**  & Power 




Results (2/2)

Reasoning Principles

- **DRF: Data Race Freedom** \Rightarrow SC 
 - DRF-PromiseFree: DRF \Rightarrow semantics w/o promises 
- **Invariant-based logic:** 
soundness of global invariant (e.g. $a=b=X=Y=0$)
- <http://sf.snu.ac.kr/promise-concurrency>



More comprehensive semantics for C/C++ concurrency

- **DRF: Data Race Freedom** \Rightarrow SC 
 - DRF-PromiseFree: DRF \Rightarrow semantics w/o promises 
- **Invariant-based logic:** 
soundness of global invariant (e.g. $a=b=X=Y=0$)
- <http://sf.snu.ac.kr/promise-concurrency>



Future Work

- Supporting **SC reads & writes**
(We found a **flaw in C/C++11 on SC**)
- Supporting **consume** reads
- Compilation to **ARMv8**
- Developing a rich **program logic & Verifying** fine-grained concurrent programs